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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,057	12/30/2003	Christopher J. Lake	42P17515	9107

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,057	LAKE ET AL.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-14,17-24 and 27-30* is/are rejected.

7)☒ Claim(s) *9-10, 15-16, 25-26, 31-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 22, 2006 has been entered.

Response to Amendment

2. This Office action is in responds to the Amendment filed on September 22, 2006, claims 1-32 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-2, 4, 17-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. (US PAT. 6,078,402 hereinafter Fischer) in view of Shariff et al. (US PAT. 5,590,374 hereinafter Shariff).

Regarding claim 1, Fischer discloses a method comprising scanning an address space to locate a structure, i.e., determining what PCI device exit and the particular configuration requirements for a new plug-in device by the configuration address space located in the configuration address register (100, figure 2) in the PCI device (65, figure 2), determining a starting address location, i.e., base address, of the structure, and accessing a register located within the structure by adding a predetermined offset to the starting location of the structure (col. 4 line 24 through col.5 line 44). Fischer differs from the claimed invention in not specifically teaches scanning an address space to locate an identification register of a structure whose value matches a predetermined value, wherein the value of the identification register identifies a starting address location of the structure within the address space. However, Shariff discloses an interface controller (32, figure 3) interactive between a host processor (12, figure 1) and plurality devices or memory modules, such as plug-in device (col. 1 lines 14-17), wherein the interface controller has a stored configuration base address for determining the unique address for which the corresponding interface module is to respond (abstract and col. 3 lines 38-41), and further comprising a identification code memory (36, figure 3), i.e., an identification register, in

responds to the read from host processor to determine the state of the requested and the configuration based address (col. 14 line 50 through col. 15 line 12), and the interface controller further determines whether the based address match the predetermine value stored in the identification code memory (36) to generate a result or whether a new configuration address needs to be generated by comparing the new configuration based address and the predetermine value stored in the identification code memory (col. 15 line 30 through col. 17 line 67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the bus interface device of Fischer in having a step of scanning an address space to locate an identification register of a structure whose value matches a predetermined value, wherein the value of the identification register identifies a starting address location of the structure within the address space, as per teaches by the interface controller of Shariff, because it eliminate all memory base address conflicts (col. 3 lines 56-60).

Regarding claims 2 and 4, Fischer discloses the method wherein scanning an address space includes scanning a PCI address space, and scanning an address space to locate a structure includes scanning an address space to locate a structure that is located within a configuration space of a device (col. 4 line 24 through col. 5 line 44).

Regarding claim 17, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claims 18 and 20, the limitations of the claims are rejected as the same reasons set forth in claims 2 and 4.

6. Claims 3, 5-8, 11-14, 19, 21-24 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer et al. (US PAT. 6,078,402 hereinafter Fischer) and Shariff et al. (US PAT. 5,590,374 hereinafter Shariff) further in view of Bland et al. (US PAT. 5,623,697 hereinafter Bland).

Regarding claim 3, the combination of Fischer and Shariff differs from the claimed invention in not specifically teaches the step of scanning an address space includes scanning a PCI express address space. However, Bland teaches a bridge chip (34, figure 2) comprising peripheral component interconnect interface (46, figure 2) interfacing to PCI bus (30, figure 2), a direct memory access controller (50, figure 2) controlling memory accesses within system (10, figure 1), and programmable input/output register (52, figure 2), i.e., configuration address register, (col. 4 lines 36-61) wherein the direct memory access controller further comprising controllers (60 and 62) produce the memory address to the PCI bus (30) with corresponding registers, i.e., low page and high page register (col. 5 lines 20-43), wherein the direct memory access controller is capable to output to different memory location based on different bits memory addressing capacity, i.e., 8-bit mode or 16-bit mode (col. 7 lines 6-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the input/output interface of the combination of Fischer and Shariff in having a method step of scanning an address space includes scanning a PCI express address space, as per teaching by the bridge chip of Bland, because it provides a compatible cycle or a faster version by selecting the values to read out of the high or low page registers during data transfers, and ensures the correct channel information is routed to the address bus, which allows incrementing and decrementing across any address boundary (col. 3 lines 42-46 and col. 9 lines 4-8).

Regarding claims 5-8, the combination of Fischer and Shariff differs from the claimed invention in not specifically teaches the step of scanning an address space to locate a structure includes reading an 8-bit PCI capabilities pointer located inside a target device, and further determining whether the 8-bit capabilities pointer is a valid capabilities pointer, wherein the 8-bit capabilities pointer to read an 8-bit capabilities identification value, and further determining whether the read capabilities identification value matches a predetermined capabilities identification value. However, Bland teaches a bridge chip (34, figure 2) comprising peripheral component interconnect interface (46, figure 2) interfacing to PCI bus (30, figure 2), a direct memory access controller (50, figure 2) controlling memory accesses within system (10, figure 1), and programmable input/output register (52, figure 2), i.e., configuration address register, (col. 4 lines 36-61) wherein the direct memory access controller further comprising controllers (60 and 62) produce the memory address to the PCI bus (30) with corresponding registers, i.e., low page and high page register (col. 5 lines 20-43), wherein both high and low page register (82 and 84) are containing the base address, i.e., starting address, and the current addresses, a up/down counter 90 resided in the direct memory access controller counts for address bits when the system boot up, and the direct memory access controller transfer and drives address bit out onto the appropriate bus (col. 9 lines 9-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the input/output interface of the combination of Fischer and Shariff in having a method step of scanning an address space to locate a structure includes reading an 8-bit PCI capabilities pointer located inside a target device, and further determining whether the 8-bit capabilities pointer is a valid capabilities pointer, wherein the 8-bit capabilities pointer to read an 8-bit capabilities identification value, and further

determining whether the read capabilities identification value matches a predetermined capabilities identification value, as per teaching by the by the bridge chip of Bland, because it provides a compatible cycle or a faster version by selecting the values to read out of the high or low page registers during data transfers, and ensures the correct channel information is routed to the address bus, which allows incrementing and decrementing across any address boundary (col. 3 lines 42-46 and col. 9 lines 4-8).

Regarding claims 11-14, the combination of Fischer and Shariff differs from the claimed invention in not specifically teaches scanning an address space to locate a structure includes reading a 12-bit PCI express capabilities pointer located inside a target device, further determining whether the 12-bit capabilities pointer is a valid capabilities pointer, and the 12-bit capabilities pointer is a valid capabilities pointer to read a 16-bit capabilities identification value, and further determining whether the read capabilities identification value matches a predetermined capabilities identification value. However, Bland teaches a bridge chip (34, figure 2) comprising peripheral component interconnect interface (46, figure 2) interfacing to PCI bus (30, figure 2), a direct memory access controller (50, figure 2) controlling memory accesses within system (10, figure 1), and programmable input/output register (52, figure 2), i.e., configuration address register, (col. 4 lines 36-61) wherein the direct memory access controller further comprising controllers (60 and 62) produce the memory address to the PCI bus (30) with corresponding registers, i.e., low page and high page register (col. 5 lines 20-43), wherein both high and low page register (82 and 84) are containing the base address, i.e., starting address, and the current addresses, a up/down counter 90 resided in the direct memory access controller counts for address bits when the system boot up, and the direct memory access controller transfer

and drives address bit out onto the appropriate bus (col. 9 lines 9-54). In addition, the difference between Bland and the claims is the claims specifically recite the PCI bus is a 12-bit bus, however, having this sized of bus does not have a disclosed purpose nor is this size disclosed to overcome any deficiencies in the prior art. S such, the PCI bus may have been of any size, and since Bland discloses a 16-bit bus capacity (col. 9 line 66 through col. 10 line 20), the ordinary artisan would realize a possible bus size increase as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the system of Bland wherein the PCI bus is 12-bit, as disclosed supra, since applicant has not disclosed that a 12-bit PCI bys, as opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the input/output interface of the combination of Fischer and Shariff in having a method step of scanning an address space to locate a structure includes reading a 12-bit PCI express capabilities pointer located inside a target device, further determining whether the 12-bit capabilities pointer is a valid capabilities pointer, and the 12-bit capabilities pointer is a valid capabilities pointer to read a 16-bit capabilities identification value, and further determining whether the read capabilities identification value matches a predetermined capabilities identification value, as per teaching by the by the bridge chip of Bland, because it provides a compatible cycle or a faster version by selecting the values to read out of the high or low page registers during data transfers, and ensures the correct channel information is routed to the address bus, which allows incrementing and decrementing across any address boundary (col. 3 lines 42-46 and col. 9 lines 4-8).

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claims 21-24, the limitations of the claims are rejected as the same reasons set forth in claims 5-8.

Regarding claims 27-30, the limitations of the claims are rejected as the same reasons set forth in claims 11-14.

Allowable Subject Matter

7. Claims 9-10, 15-16, 25-26 and 31-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 1-32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lee et al. (US PAT. 6,973,526) discloses method and apparatus to permit external access to internal configuration registers (abstract).

Moy (US PAT. 6,820,149) discloses method, system and program for testing a bus interface wherein the bus interface is configured with base addresses that enable transmission of I/O request over the bus to the memory (col. 2 lines 3-59).

Melo et al. (US PAT. 6,241,400) discloses configuration logic within a PCI compliant bus interface unit, which can be selectively disconnected from a clocking source to conserve power (abstract).

Porterfield (US PAT. 6,587,868) discloses computer system having peer-to-peer bus bridges and shadow configuration registers (col. 2 lines 28-58).

Bennett et al. (US Pub. 2003/0,188,122) discloses mapping of interconnect configuration space (abstract).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Zhuo H. Li

Patent Examiner
November 7, 2006

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